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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,831	12/30/2003	Kevin M. Conley	SNDK.247US0	9380

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
06/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,831	CONLEY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 April 2007 has been entered.

Status of Claims

2. Claims 2-4 and 26-35 are pending in the Application.

Claims 1 and 5-25 remain cancelled.

Claims 31-35 are new.

Claims 2-4 and 26-30 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 26 April 2007 in response to the office action mailed on 26 October 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 26 April 2007 was fully considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2-4, 28, 29, 31, 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US PG Publication 2002/0099904 A1).

As for claim 2 (and 28), Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

responding to host commands to write units of data having non-sequential logical addresses by writing the data with sequential physical addresses into a first designated block (or a number of sequential logical addresses less than a fraction of said given number as in claim 28), and responding to host commands to write units of data having sequential logical addresses equal to or in excess of a given proportion (or the fraction of claim 28) of said given number by writing the data into a second designated block (paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of

the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages)).

Also note Conley's system is designed to account for storing either sequential logically addressed data, or non-sequentially logically addressed data, as described in paragraph 0050, all lines. In other words, if the given amount of host data is smaller than the area remaining in a partially written block, it will be stored in the first block (regardless if the data has sequential or non-sequential logical address). If the data is excess of a proportion of that given amount (amount of memory available in the partial block), the data will be written to the second, newly allocated block, again irrespective of the sequence of the logical addresses. More specifically, the mapping of data can be for contiguous (i.e. sequential) logical addresses as discussed in paragraph 0042 (i.e. mapping logical block pages 0-7 to physical block pages 0-7), or non-sequential logical addresses as per paragraph 0007 (writing fewer than all pages by only writing pages the same logical address, and/or writing pages that only have been changed (rather than being forced to write all contiguous logical addresses even if some of those addresses have not been updated)).

As for claim 31, Conley teaches a method of operating a non-volatile memory system in response to commands received from a host to individually write logically addressed units of data therein, the memory system having memory cells grouped into

blocks that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, comprising:

allocating a first one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number (Fig. 14, elements 52, 53, 61, 63 – paragraph 0062 – if the system determines that enough space is available to accommodate the amount of data required by the pages corresponding to a number of logical addresses, the data will be allocated to the partially written block),

allocating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number (Fig. 14, elements 52, 53, 55 – paragraph 0062 – if the system determines if a sufficient amount of space is not available to accommodate the amount of data required by the pages corresponding to the number of logical addresses, a second block (new erased block) will be allocated to store the data),

in response to receipt of a command to write data having a number of sequential logical addresses less than said fraction, determining whether the first block has sufficient erased capacity to store the received data and, if so, writing the received data into sequential physical addresses of the first block (Fig. 14, elements 61 and 67 – paragraph 0062 – once the system determines that enough pages are available in the

partially written block (i.e. element 61), the data will be written into the newly allocated block (element 67)), and

in response to receipt of a command to write data having a number of sequential logical addresses equal to or in excess of said fraction, determining whether the second block has erased capacity to store the data and, if so, writing the data into sequential physical addresses of the second block (Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a new erased block is sufficient to store the data, the new data is written to the block (element 57)).

As for claim 32, Conley teaches,

in response to receipt of the command to write data having a number of sequential logical addresses less than said fraction, if the first block does not have sufficient erased capacity to store the received data, allocating a third one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number and then writing the received data into sequential physical addresses of the third block (Fig. 14, elements 65 and 67 – paragraph 0062 – once the system determines that the partial block is not large enough, a new erased block (third) will be allocated and written to), and

in response to receipt of the command to write data having a number of sequential logical addresses equal to or in excess of said fraction, if the second block does not have sufficient erased capacity to store the received data, allocating a fourth one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number and then writing the received

data into sequential physical addresses of the fourth block (Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a one new erased block is not sufficient to store the data, an additional block (i.e. fourth) will be allocated to accommodate the new data (elements 55 and 57)).

As for claim 3, Conley teaches writing data to the first designated block as including writing a number of host units of data into the first designated block having sequential logical addresses less than the given proportion of said given number (referring again to paragraph 0062, the given number is based on the memory available within the partial block).

As for claims 4, 29 and 34, Conley teaches the non-volatile memory cells as being organized into multiple sub-arrays, and said blocks of memory cells include memory cells of two or more of the sub-arrays (paragraph 0062, all lines, if the amount of host data does not exceed the size of one full block the data, two different sets of host writes can be stored uniquely in one block (i.e. each write is a unique sub-array of data within each block). Also note Conley specifically teaches his memory system as including sub-arrays in paragraph 0010, lines 1-7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 26, 27, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (US PG Publication 2002/0099904 A1) as applied to claims 2 and 28 above, and in further view of Kulkarni et al. (Us PG Publication 2002/0034105 A1), hereinafter Kulkarni.

As for claims 26, 27, 30, 33 and 35 though Conley teaches all the limitations of claims 2 and 28, he fails to specifically teach the given proportion as being set within a range of 25-75 percent of the given number as recited by Applicant in these claims.

Kulkarni however teaches a system and method for incrementally updating an image in flash memory wherein new flash images are built incrementally until a memory block is of sufficient size to be written to the flash memory – paragraph 0013, all lines. More specifically, Kulkarni teaches writing memory to a first memory block (i.e. RAM), until the memory is half full (i.e. 50 percent), and subsequently writing the data to a second block in the flash memory (i.e. predetermined limit set at 50% allocation) – paragraph 0014, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Conley to further include Kulkarni's system for updating an image in flash memory into his own system for partial block data programming in a non-volatile memory. By doing so, Conley would have a more efficient memory system capable for reducing the number of sections transmitted during the writing process, while persevering sections that are used to construct other section as taught by Kulkarni in paragraph 0011, all lines. Additionally, Conley could benefit from Kulkarni's system by

preventing the problems related to data overwrite as described by Kulkarni in paragraph 0012, all lines.

Response to Arguments

7. Applicant's amendments and arguments with respect to the claims rejected under the 35 USC § 102(b) have been fully considered, but they are not persuasive (i.e. claims 2-4, 28 and 29).

8. With respect to the rejections set forth under 35 USC § 102(b), Applicant asserts, "[t]he application of the Conley reference in the final Office Action appears to be equating logical addresses of data received from a host with the physical addresses of the memory at which the received data are stored, which, if this is being correctly understood, is believed to be incorrect." Applicant further contends, "[b]ut what is respectfully submitted to be incorrect is equating this [Conley's cited paragraph 0062] with selecting a physical block in which received data are to be written based upon the number of sequential logical addresses of the received data, as is claimed." Applicant further attempts to contrast Conley with figures and disclosures as per the original specification (i.e. describes the memory system translating received logical addresses into physical addresses). Applicant concludes by stating, "Conley's choice of a memory cell block based on its physical capability to store received data is respectfully submitted to be much different from and not to anticipate the claimed use of a number of sequential logical addresses of the received data to make the block choice."

This argument however is not persuasive. More specifically, Conley clearly discloses a correspondence between logical and physical addresses (i.e. Figs. 5A, 5B, 7A, 7B, 8, 9, 12). In fact, Conley specifically speaks to the mapping of logical to physical addresses/blocks in paragraph 0042 of his disclosure. The mapping of data can be for contiguous (i.e. sequential) logical addresses as discussed in paragraph 0042 (i.e. mapping logical block pages 0-7 to physical block pages 0-7), or non-sequential logical addresses as per paragraph 0007 (writing fewer than all pages by only writing pages the same logical address, and/or writing pages that only have been changed (rather than being forced to write all contiguous logical addresses even if some of those addresses have not been updated)). Further, since the physical and logical addresses correspond directly to a fixed amount of data (more specifically, a page), Conley's system determines if it is to write to a new block based on the number logical addresses. For example, if a partial block has the capacity to store four pages, the system will allocate the "at least one new erased block" if the data referenced by five or more logical addresses are to be written (see Fig.14, elements 53 and 55). In other words, the system's determination to store the data in a newly erased block directly corresponds to the number of logical addresses referencing the data to be stored.

9. With respect to the rejections set forth under 35 USC § 103(a), Applicant contends the rejection is improper for the same reasons stated above for the parent claim (incidentally, this is not persuasive as per the rebuttal argument and rejection, *supra*), and additionally because "Kulkarni describes a completely different process than that being claimed." With respect to the latter argument, Applicant asserts, "[Kulkarni

describes a] different process, with a different purpose, than that being claimed is respectfully submitted not to have rendered obvious the use of the claimed 25-75 proportion (or fraction) of the capacity of a memory cell block to make the decision of which memory cell block the data will be written to. Kulkarni uses this percentage breakpoint to decide when to write accumulating data into flash memory, not to decide which of at least two blocks data will be written, as claimed."

This argument however is not persuasive. More specifically, pursuant to MPEP § 2145 (IV.), Applicant is reminded, "[o]ne cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant attempts to attack the Kulkarni reference, rather than addressing whether or not it would have been obvious for Conley to modify his teachings to allocate different blocks based on a threshold as per Kulkarni's teachings. Since Applicant has failed to sufficiently rebut Examiner's properly established prima *facie* case of obviousness, the argument is not persuasive, and the rejection is deemed proper.

10. Applicant arguments with respect to the newly added claims are not persuasive, as Examiner maintains that Conley renders each of these claims either anticipated and/or obvious as per the rejections and arguments presented *supra*.

Conclusion

11. This is a Request for Continued Examination. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

GARY PORTKA
PRIMARY EXAMINER